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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,127	01/30/2004	Ping Mei	200209576-1	8740

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EXAMINER	
TRAN, THANH Y	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/769,127	MEI, PING	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *11,12,21 and 24-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 13-20, 22-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10, 13-20, and 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Taussig et al (U.S. 6,861,365).

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As to claim 1, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device comprising: forming a 3-dimensional (3D) pattern (212) in a substrate (410); and depositing at least one material (214/420) over the substrate (410) in accordance with desired characteristics of the semiconductor device (see col. 2, lines 12-20).

As to claim 2, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein forming the 3D pattern (212) further comprises: depositing a layer of material (214/420) onto the substrate (410); imprinting a 3D pattern (212) into the layer

of material (214/420) (see col. 1, lines 24-35); and transferring the 3D pattern into the substrate (see col. 2, lines 12-20).

As to claims 3 and 14, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein the semiconductor device comprises a cross-point memory array (see col. 3, lines 61-67).

As to claims 4 and 17, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein the semiconductor device is at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse (see claim 8 and col. 4, lines 14-20).

As to claim 5, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein imprinting a 3D pattern into the layer of material (214/420) further comprises utilizing a 3D stamping tool (210) to create the 3D pattern (212) (see col. 2, lines 30-31).

As to claim 6, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein imprinting a 3D pattern into the layer of material (214/420) further comprises utilizing a molding process to imprint the 3D pattern into the layer of material (214/420) (see col. 1, line 60 – col. 2, line 5; and col. 3, lines 1-7).

As to claims 7, and 22, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein the layer of material comprises a polymer material (see col. 3, lines 30-43).

As to claims 8, and 23, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein the layer of material comprises a photo-resist material ("resist structure"/"resist layer" 420/214) (see col. 3, lines 52-60; and col. 4, lines 44-51).

As to claim 9, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein transferring the 3D pattern into the substrate includes: removing a portion of the layer of material (214/420) thereby exposing a portion of the substrate (410) (see figures 4a-4d); etching the exposed portion of the substrate (410) (see figure 4c, and claim 9); removing another portion of the layer of material (214/420) thereby exposing a second portion of the substrate (see figures 4a-4d; and col. 4, line 66 - col. 5, line 5); etching the second portion of the substrate (410) (see figures 4a-4d); and removing a remaining portion of the layer of material (214/420) (see figures 4c-4d).

As to claim 10, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a method for forming a semiconductor device, wherein depositing at least one material over the substrate further comprises: depositing two sets of conductors with a semiconductor layer a there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place (see col. 3, lines 61-67).

As to claim 13, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a system for forming a semiconductor device comprising: means (210) for forming a pattern (212) in a substrate wherein the pattern is 3-dimensional (see col. 2, lines 12-20); and means for depositing at least one semiconductor material (214/420) over the substrate (410) in accordance with desired characteristics of the semiconductor device (see col. 2, lines 12-20).

As to claim 15, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a system for forming a semiconductor device, wherein the means for forming the pattern (212) further comprises: means for depositing a layer of material (214/420) onto the substrate (410) (col. 2, lines 12-20); means for imprinting a 3D pattern (212) onto the layer of material (214/420) (see figure 2a, and

col. 1, lines 24-35); and means for transferring the 3D pattern into the substrate (see col. 2, lines 12-20).

As to claim 16, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a system for forming a semiconductor device, wherein the means for depositing at least one semiconductor material over the substrate further comprises: means for depositing two sets of conductors with a semiconductor layer there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place (see col. 3, lines 61-67).

As to claim 18, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a system for forming a semiconductor device, wherein the means for imprinting a 3D pattern into the layer of material (214/420) further comprises means for implementing a molding process to imprint the 3D pattern into the layer of material (214/420) (see col. 1, line 60 – col. 2, line 5; and col. 3, lines 1-7).

As to claim 19, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a system for forming a semiconductor device, wherein the means for transferring the 3D pattern into the substrate includes: means for removing a portion of the layer of material (214/420) thereby exposing a portion of the substrate (410) (see figures 4a-4d); means for etching the exposed portion of the substrate (410) (see figure 4c, and claim 9); means for removing another portion of the layer of material (214/420) thereby exposing a second portion of the substrate (see figures 4a-4d; and col. 4, line 66 - col. 5, line 5); means for etching the second portion of the substrate (see figures 4c-4d); and means for removing a remaining portion of the layer of material (420) (see figures 4c-4d).

As to claim 20, Taussig et al discloses in figures 1, 2a-2b, and 4a-5 a system for forming a semiconductor device, wherein the means for imprinting a 3D pattern onto the layer of material (214/420) further comprises means for utilizing a 3D stamping tool (210) to create the 3D pattern (212) (see col. 2, lines 30-31).

Response to Arguments

3. Applicant argued that Taussig reference does not disclose forming a 3-dimensional (3D) pattern in a substrate as recited in claim 1.

In response, the examiner disagrees with applicant's argument because Taussig reference clearly discloses in figure 1 the step of forming a 3-dimensional (3D) pattern (see step 130) in a substrate (see step 110) (also see col. 3, lines 14-30).

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Michael Trinh
Primary Examiner
1/22/07